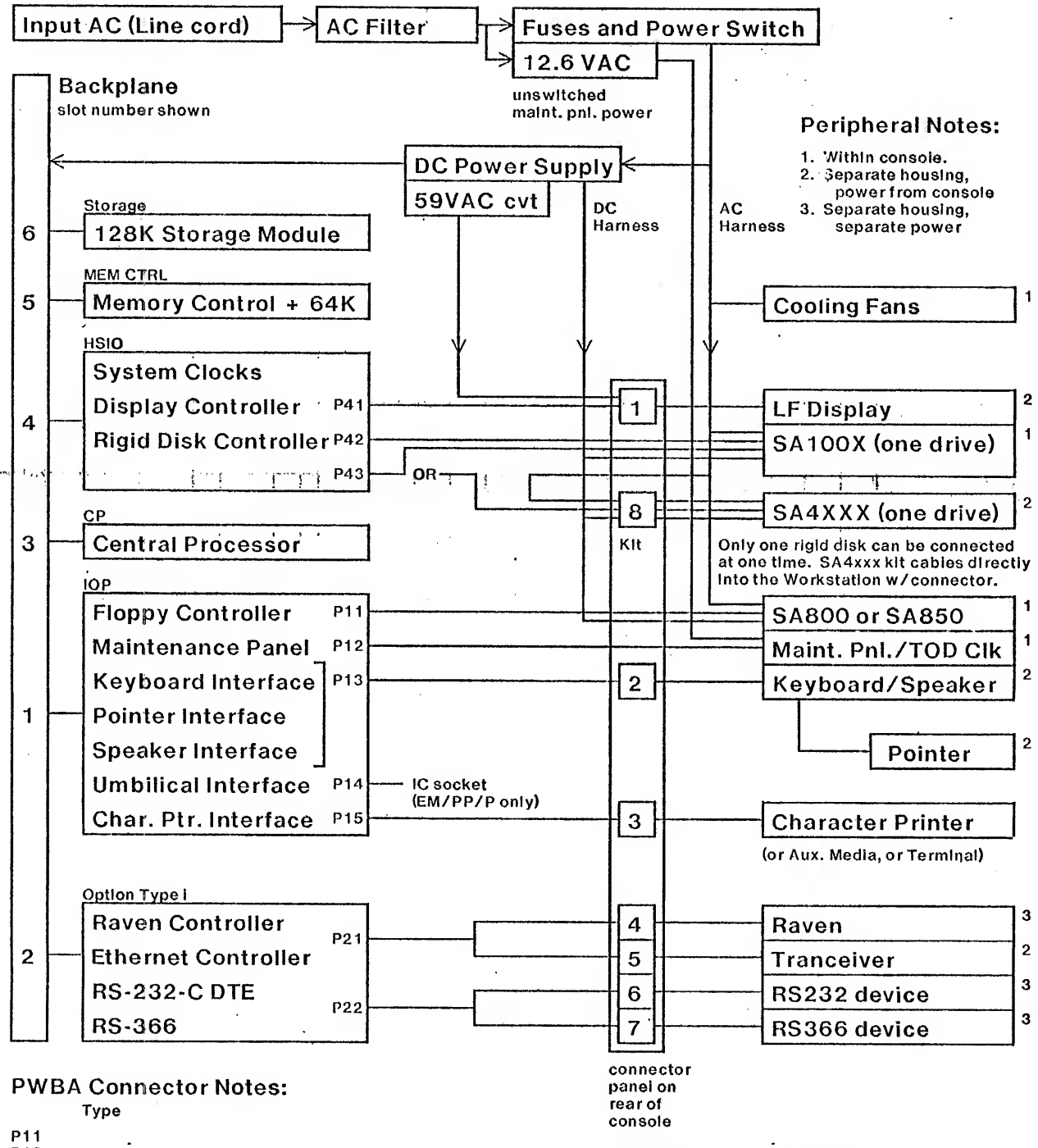
<= =<<

# Workstation Configuration

## Base Line Workstation

June 1, 1980 RLB
ws-config.sil




## PWBA Connector Notes:

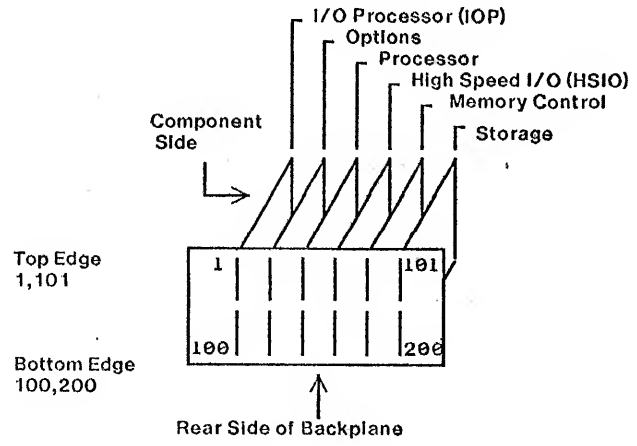
| | Type |
|---|---|
| P11 | |
| P12 | |
| P13 | 713W12720 (XEROX) 40 POS. |
| P14 | 20 PIN I.C. SOCKET |
| P15 | 713W12220 (XEROX) 10 POS. |
| P21 | 713W12720 (XEROX) 40 POS. |
| P22 | 713W12820 (XEROX) 50 POS. |
| P41 | 713W12220 (XEROX) 10 POS. |
| P42 | |
| P43 | |

## Connector Panel Notes:

| | |
|---|---|
| 1 | D Series 25 Pin Socket |
| 2 | D Series 50 Pin Socket |
| 3 | D Series 25 Pin Socket |
| 4 | D Series 25 Pin Plug |
| 5 | D Series 25 Pin Socket |
| 6 | D Series 25 Pin Socket |
| 7 | D Series 25 Pin Socket |
| 8 | Kit |

# Dandelion Backplane

## Physical arrangement




## Files

[Iris]<Workstation>Backplane>
Backplane-B.press
Backplane-B.dm

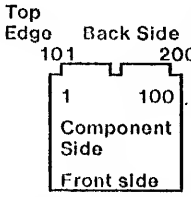
## Backplane Signals

| Card | IOP | Options | Central Processor | High Speed I/O | Memory Control | Storage |
|---|---|---|---|---|---|---|
| Total Signal lines used | 131 | 166 | 140 | 141 | 155 | 66 |
| I/O Connectors on front of boards | Floppy<br>Keyboard<br>Printer<br>MaintenanceP<br>Alto umb. | LSEP/Ethernet<br>RS232/RS366 | | SA4XXX<br>SA100X<br>Display | | |

170 max. per card

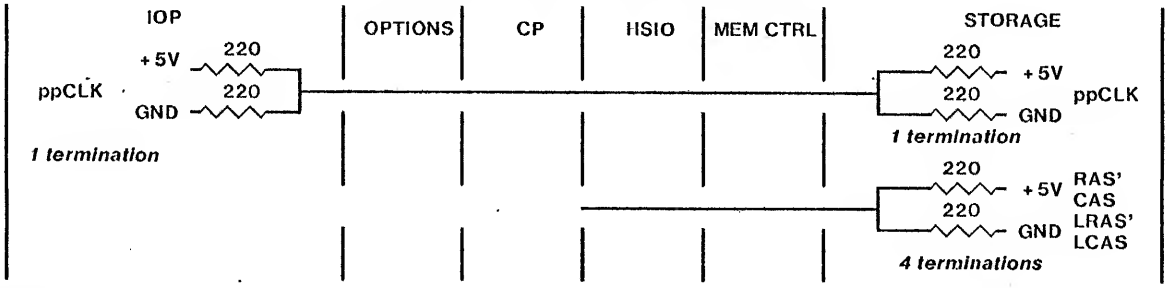
## Power distribution

| Backplane Power & Ground | 30 lines total |
|---|---|
| Voltage | Backplane Pins |
| + 12 V | 1,101 |
| + 5 V | 50,51,150,151 |
| Gnd | 10,20,30,40,60,70,80,90,110,120,130,140,160,170,180,190 |
| - 5V | 100,200 |
| - 12 V | 98,198 |
| No Conn. | 97,99,197,199 |




2- 100 pin connectors
Pins on .1" centers
.6" between pins 50 & 51
AMP # 530826-3

## Termination of clock signals




Terminations are placed on the IOP and STORAGE cards.

| XEROX SDD | Project | Backplane Description | File | Designer | Rev | Date |
|---|---|---|---|---|---|---|
| | Dandelion | General Characteristics | WSBackplane.sil | Ogus | B | 2/19/80 |

| | IOP | | OPTIONS | | CP | | HSIO | | |
|---|---|---|---|---|---|---|---|---|---|
| 02 | | | 02 Cycle.1' | Click.0 | 02 Cycle1' | Click.0 | 02 Cycle1' | Click.0 | 02 |
| 03 | | | 03 Cycle.2' | Click.1 | 03 Cycle2' | Click.1 | 03 Cycle2' | Click.1 | 03 |
| 04 | | | 04 Cycle.3' | Click.2 | 04 Cycle3' | Click.2 | 04 Cycle3' | Click.2 | 04 |
| 05 | Spare22 | Spare23 | 05 Spare22 | Spare23 | 05 | | 05 RAS' | LRAS' | 05 |
| 06 | IOPALE | | 06 IOPALE | | 06 | | 06 CAS | LCAS | 06 |
| 07 | Spare20 | Spare21 | 07 Spare20 | Spare21 | 07 Spare20 | Spare21 | 07 WPulse | DR/C | 07 |
| 08 | Spare18 | Spare19 | 08 Spare18 | Spare19 | 08 Spare18 | Spare19 | 08 | | 08 |
| 09 | ppCLK | | 09 ppCLK | | 09 ppCLK | | 09 ppCLK | | 09 |
| 11 | Spare16 | Spare17 | 11 Spare16 | Spare17 | 11 AllowWrite | | 11 AllowWrite | | 11 |
| 12 | IOPClk | | 12 IOPClk | | 12 | | 12 | | 12 |
| 13 | Spare14 | Spare15 | 13 Spare14 | Spare15 | 13 MAR← | mem | 13 MAR← | mem | 13 |
| 14 | Spare12 | Spare13 | 14 Spare12 | Spare13 | 14 | ←MStatus' | 14 | ←MStatus' | 14 |
| 15 | Spare10 | Spare11 | 15 Spare10 | Spare11 | 15 MapRef | MCtl←' | 15 MapRef | MCtl←' | 15 |
| 16 | SelTroyMode | Spare9 | 16 SelTroyMode | Spare9 | 16 Refresh' | | 16 Refresh' | | 16 |
| 17 | Wait | IOPReset' | 17 Wait | IOPReset' | 17 Wait | IOPReset' | 17 Wait | IOPReset' | 17 |
| 18 | TrIndex | TrHdLd | 18 TrIndex | TrHdLd | 18 Spare26 | Spare27 | 18 Spare26 | Spare27 | 18 |
| 19 | TrReady | TrStep | 19 TrReady | TrStep | 19 Spare24 | Spare25 | 19 Spare24 | Spare25 | 19 |
| 21 | IOPODate←' | IOPCtl←' | 21 IOPODate←' | IOPCtl←' | 21 IOPODate←' | IOPCtl←' | 21 | | 21 |
| 22 | TrTK00 | TrDirIn | 22 TrTK00 | TrDirIn | 22 KOData←' | KCtl←' | 22 KOData←' | KCtl←' | 22 |
| 23 | | | 23 XOData←' | XCtl←' | 23 XOData←' | XCtl←' | 23 XOData←' | XCtl←' | 23 |
| 24 | TrWrProt | TrWrGate | 24 TrWrProt | TrWrGate | 24 DCtlFIfo←' | DCtl←' | 24 DCtlFifo←' | DCtl←' | 24 |
| 25 | TrRdData | TrWrData | 25 TrRdData | TrWrData | 25 DBorder←' | | 25 DBorder←' | | 25 |
| 26 | IOOutSp1←' | IOOutSp2←' | 26 IOOutSp1←' | IOOutSp2←' | 26 IOOutSp1←' | IOOutSp2←' | 26 IOOutSp1←' | IOOutSp2←' | 26 |
| 27 | IOOutSp3←' | IOOutSp4←' | 27 IOOutSp3←' | IOOutSp4←' | 27 IOOutSp3←' | IOOutSp4←' | 27 IOOutSp3←' | IOOutSp4←' | 27 |
| 28 | | | 28 POData←' | PCtl←' | 28 POData←' | PCtl←' | 28 POData←' | PCtl←' | 28 |
| 29 | Spare6 | Spare7 | 29 Spare6 | Spare7 | 29 Spare6 | Spare7 | 29 Spare6 | Spare7 | 29 |
| 31 | | | 31 ←XIData' | ←XStatus' | 31 ←XIData' | ←XStatus' | 31 ←XIData' | ←XStatus' | 31 |
| 32 | Spare4 | Spare5 | 32 Spare4 | Spare5 | 32 ←KIData' | ←KStatus' | 32 ←KIData' | ←KStatus' | 32 |
| 33 | | | 33 | ←PStatus' | 33 ←KTest' | ←PStatus' | 33 ←KTest' | ←PStatus' | 33 |
| 34 | ←IOPIData' | ←IOPStatus' | 34 ←IOPIData' | ←IOPStatus' | 34 ←IOPIData' | ←IOPStatus' | 34 | | 34 |
| 35 | ←IOInSp2' | | 35 ←IOInSp2' | ClrRefReq' | 35 ←IOInSp2' | ClrRefReq' | 35 ←IOInSp2' | ClrRefReq' | 35 |
| 36 | Spare2 | Spare3 | 36 Spare2 | Spare3 | 36 Spare2 | Spare3 | 36 Spare2 | Spare3 | 36 |
| 37 | CSParErr | | 37 CSParErr | EndLine' | 37 CSParErr | EndLine' | 37 | EndLine' | 37 |
| 38 | IODisp.0 | IODisp.1 | 38 IODisp.0 | IODisp.1 | 38 IODisp.0 | IODisp.1 | 38 IODisp.0 | IODisp.1 | 38 |
| 39 | YIODisp.0 | YIODisp.1 | 39 YIODisp.0 | YIODisp.1 | 39 YIODisp.0 | YIODisp.1 | 39 YIODisp.0 | YIODisp.1 | 39 |
| 41 | X.0 | X.1 | 41 X.0 | X.1 | 41 X.0 | X.1 | 41 X.0 | X.1 | 41 |
| 42 | X.2 | X.3 | 42 X.2 | X.3 | 42 X.2 | X.3 | 42 X.2 | X.3 | 42 |
| 43 | X.4 | X.5 | 43 X.4 | X.5 | 43 X.4 | X.5 | 43 X.4 | X.5 | 43 |
| 44 | X.6 | X.7 | 44 X.6 | X.7 | 44 X.6 | X.7 | 44 X.6 | X.7 | 44 |
| 45 | X.8 | X.9 | 45 X.8 | X.9 | 45 X.8 | X.9 | 45 X.8 | X.9 | 45 |
| 46 | X.10 | X.11 | 46 X.10 | X.11 | 46 X.10 | X.11 | 46 X.10 | X.11 | 46 |
| 47 | X.12 | X.13 | 47 X.12 | X.13 | 47 X.12 | X.13 | 47 X.12 | X.13 | 47 |
| 48 | X.14 | X.15 | 48 X.14 | X.15 | 48 X.14 | X.15 | 48 X.14 | X.15 | 48 |
| 49 | | | 49 Y.0 | Y.1 | 49 Y.0 | Y.1 | 49 Y.0 | Y.1 | 49 |
| 52 | | | 52 Y.2 | Y.3 | 52 Y.2 | Y.3 | 52 Y.2 | Y.3 | 52 |
| 53 | | | 53 Y.4 | Y.5 | 53 Y.4 | Y.5 | 53 Y.4 | Y.5 | 53 |
| 54 | | | 54 Y.6 | Y.7 | 54 Y.6 | Y.7 | 54 Y.6 | Y.7 | 54 |
| 55 | | | 55 Y.8 | Y.9 | 55 Y.8 | Y.9 | 55 Y.8 | Y.9 | 55 |
| 56 | | | 56 Y.10 | Y.11 | 56 Y.10 | Y.11 | 56 Y.10 | Y.11 | 56 |
| 57 | | | 57 Y.12 | Y.13 | 57 Y.12 | Y.13 | 57 Y.12 | Y.13 | 57 |
| 58 | | | 58 Y.14 | Y.15 | 58 Y.14 | Y.15 | 58 Y.14 | Y.15 | 58 |
| 59 | DmaReqC | DmaAckC | 59 DmaReqC | DmaAckC | 59 YH.0 | YH.1 | 59 YH.0 | YH.1 | 59 |
| 61 | DmaReqA | DmaAckA | 61 DmaReqA | DmaAckA | 61 YH.2 | YH.3 | 61 YH.2 | YH.3 | 61 |
| 62 | DmaReqB | DmaAckB | 62 DmaReqB | DmaAckB | 62 YH.4 | YH.5 | 62 YH.4 | YH.5 | 62 |
| 63 | DmaCycle | ExtWaitReq' | 63 DmaCycle | ExtWaitReq' | 63 YH.6 | YH.7 | 63 YH.6 | YH.7 | 63 |
| 64 | IOPIntReq0 | IOPIntReq1 | 64 IOPIntReq0 | IOPIntReq1 | 64 Pt.0 | Pt.1 | 64 Pt.0 | Pt.1 | 64 |
| 65 | IOPIntReq2 | IOPIntReq3 | 65 IOPIntReq2 | IOPIntReq3 | 65 Pt.2 | | 65 Pt.2 | | 65 |
| 66 | IOPSel.0 | IOPSel.1 | 66 IOPSel.0 | IOPSel.1 | 66 Disp-Proc' | MemErr | 66 Disp-Proc' | MemErr | 66 |
| 67 | IOPSel.2 | IOPSel.3 | 67 IOPSel.2 | IOPSel.3 | 67 | | 67 DAddr.0 | DAddr.1 | 67 |
| 68 | IOPSel.4 | IOPSel.5 | 68 IOPSel.4 | IOPSel.5 | 68 | | 68 DAddr.2 | DAddr.3 | 68 |
| 69 | IOPAddr.00 | IOPAddr.01 | 69 IOPAddr.00 | IOPAddr.01 | 69 | | 69 DAddr.4 | DAddr.5 | 69 |
| 71 | IOPAddr.02 | IOPAddr.03 | 71 IOPAddr.02 | IOPAddr.03 | 71 | | 71 DAddr.6 | DAddr.7 | 71 |
| 72 | IOPAddr.04 | IOPAddr.05 | 72 IOPAddr.04 | IOPAddr.05 | 72 | | 72 DAddr.8 | DAddr.9 | 72 |
| 73 | IOPAddr.06 | IOPAddr.07 | 73 IOPAddr.06 | IOPAddr.07 | 73 | | 73 DAddr.10 | DAddr.11 | 73 |
| 74 | IOPAddr.08 | IOPAddr.09 | 74 IOPAddr.08 | IOPAddr.09 | 74 | | 74 DAddr.12 | DAddr.13 | 74 |
| 75 | IOPAddr.10 | IOPAddr.11 | 75 IOPAddr.10 | IOPAddr.11 | 75 | | 75 DAddr.14 | DAddr.15 | 75 |
| 76 | IOPAddr.12 | IOPAddr.13 | 76 IOPAddr.12 | IOPAddr.13 | 76 IOPAddr.12 | IOPAddr.13 | 76 DData.0 | DData.1 | 76 |
| 77 | IOPAddr.14 | IOPAddr.15 | 77 IOPAddr.14 | IOPAddr.15 | 77 IOPAddr.14 | IOPAddr.15 | 77 DData.2 | DData.3 | 77 |
| 78 | Spare0 | Spare1 | 78 Spare0 | Spare1 | 78 Spare0 | Spare1 | 78 DData.4 | DData.5 | 78 |
| 79 | IOPMemRd' | IOPI/ORd' | 79 IOPMemRd' | IOPI/ORd' | 79 | | 79 DData.6 | DData.7 | 79 |
| 81 | CSWE.a' | CSWE.b' | 81 CSWE.a' | CSWE.b' | 81 CSWE.a' | CSWE.b' | 81 DData.8 | DData.9 | 81 |
| 82 | CSWE.c' | CSWE.d' | 82 CSWE.c' | CSWE.d' | 82 CSWE.c' | CSWE.d' | 82 DData.10 | DData.11 | 82 |
| 83 | CSWE.e' | CSWE.f' | 83 CSWE.e' | CSWE.f' | 83 CSWE.e' | CSWE.f' | 83 DData.12 | DData.13 | 83 |
| 84 | IOPReq' | ClrIOPReq' | 84 IOPReq' | ClrIOPReq' | 84 IOPReq' | ClrIOPReq' | 84 DData.14 | DData.15 | 84 |
| 85 | | | 85 DPReq' | ClrDPReq' | 85 DPReq' | ClrDPReq' | 85 DPReq' | ClrDPReq' | 85 |
| 86 | | | 86 XReq' | ClrXReq' | 86 XReq' | ClrXReq' | 86 XReq' | ClrXReq' | 86 |
| 87 | IOPMemWr' | IOPI/OWr' | 87 IOPMemWr' | IOPI/OWr' | 87 KReq' | ClrKFlags' | 87 KReq' | ClrKFlags' | 87 |
| 88 | RefReq' | ReadCSEn' | 88 RefReq' | ReadCSEn' | 88 RefReq' | ReadCSEn' | 88 RefReq' | | 88 |
| 89 | SpareReq' | IOPWait | 89 SpareReq' | IOPWait | 89 SpareReq' | IOPWait | 89 SpareReq' | | 89 |
| 91 | WrTPCHigh' | WrTPCLow | 91 WrTPCHigh' | WrTPCLow | 91 WrTPCHigh' | WrTPCLow | 91 | | 91 |
| 92 | IOPData.0 | IOPData.1 | 92 IOPData.0 | IOPData.1 | 92 IOPData.0 | IOPData.1 | 92 | | 92 |
| 93 | IOPData.2 | IOPData.3 | 93 IOPData.2 | IOPData.3 | 93 IOPData.2 | IOPData.3 | 93 | | 93 |
| 94 | IOPData.4 | IOPData.5 | 94 IOPData.4 | IOPData.5 | 94 IOPData.4 | IOPData.5 | 94 | | 94 |
| 95 | IOPData.6 | IOPData.7 | 95 IOPData.6 | IOPData.7 | 95 IOPData.6 | IOPData.7 | 95 | | 95 |
| 96 | SwTAddr | SwTAddr' | 96 SwTAddr | SwTAddr' | 96 SwTAddr | SwTAddr' | 96 | | 96 |
| | 1-100 | 101-200 | 1-100 | 101-200 | 1-100 | 101-200 | 1-100 | 101-200 | |

Above diagram is rear view (wiring side) of backplane.
ALL NUMBERS ARE IN DECIMAL.

# Dandelion Backplane Signals - 1

Stamen1-4.sil in: [Iris]<Workstation>Backplane>Backplane-B.dm

| Rev B | 2/19/80 |
|---|---|
| Ogus | 1:17 p |

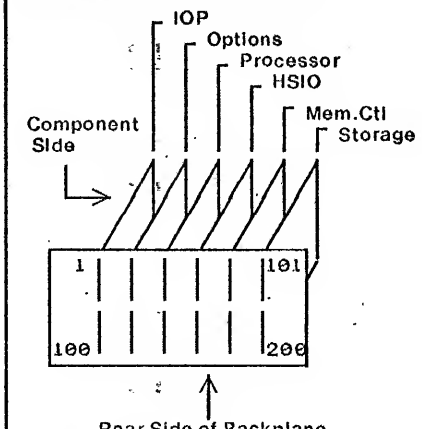
| | MEM CTRL | | | STORAGE | | |
|---|---|---|---|---|---|---|
| 02 | Cycle1' | | 02 | | | 02 |
| 03 | Cycle2' | | 03 | | | 03 |
| 04 | Cycle3' | | 04 | | | 04 |
| 05 | RAS' | LRAS' | 05 | RAS' | LRAS' | 05 |
| 06 | CAS | LCAS | 06 | CAS | LCAS | 06 |
| 07 | WPulse | DR/C | 07 | | | 07 |
| 08 | | | 08 | | | 08 |
| 09 | ppCLK | | 09 | ppCLK | | 09 |
| 11 | AllowWrite | | 11 | | | 11 |
| 12 | Bank0' | | 12 | Bank0' | | 12 |
| 13 | MAR← | mem | 13 | | | 13 |
| 14 | | ←MStatus' | 14 | | | 14 |
| 15 | MapRef | MCtl← | 15 | | | 15 |
| 16 | Refresh' | CRefresh' | 16 | Refresh' | CRefresh' | 16 |
| 17 | Wait | | 17 | | | 17 |
| 18 | SDO.00 | SDO.01 | 18 | SDO.00 | SDO.01 | 18 |
| 19 | SDO.02 | SDO.03 | 19 | SDO.02 | SDO.03 | 19 |
| 21 | SDO.04 | SDO.05 | 21 | SDO.04 | SDO.05 | 21 |
| 22 | SDO.06 | SDO.07 | 22 | SDO.06 | SDO.07 | 22 |
| 23 | SDO.08 | SDO.09 | 23 | SDO.08 | SDO.09 | 23 |
| 24 | SDO.10 | SDO.11 | 24 | SDO.10 | SDO.11 | 24 |
| 25 | SDO.12 | SDO.13 | 25 | SDO.12 | SDO.13 | 25 |
| 26 | SDO.14 | SDO.15 | 26 | SDO.14 | SDO.15 | 26 |
| 27 | SDO.16 | SDO.17 | 27 | SDO.16 | SDO.17 | 27 |
| 28 | SDO.18 | SDO.19 | 28 | SDO.18 | SDO.19 | 28 |
| 29 | SDO.20 | SDO.21 | 29 | SDO.20 | SDO.21 | 29 |
| 31 | | | 31 | | | 31 |
| 32 | SAddr.00 | SAddr.01 | 32 | SAddr.00 | SAddr.01 | 32 |
| 33 | SAddr.02 | SAddr.03 | 33 | SAddr.02 | SAddr.03 | 33 |
| 34 | SAddr.04 | SAddr.05 | 34 | SAddr.04 | SAddr.05 | 34 |
| 35 | SAddr.06 | SAddr.07 | 35 | SAddr.06 | SAddr.07 | 35 |
| 36 | Y1Latch | YOLatch | 36 | Y1Latch | YOLatch | 36 |
| 37 | Bank1' | Bank2' | 37 | Bank1' | Bank2' | 37 |
| 38 | MRef' | Write' | 38 | MRef' | Write' | 38 |
| 39 | | | 39 | | | 39 |
| 41 | X.0 | X.1 | 41 | | | 41 |
| 42 | X.2 | X.3 | 42 | | | 42 |
| 43 | X.4 | X.5 | 43 | | | 43 |
| 44 | X.6 | X.7 | 44 | | | 44 |
| 45 | X.8 | X.9 | 45 | | | 45 |
| 46 | X.10 | X.11 | 46 | | | 46 |
| 47 | X.12 | X.13 | 47 | | | 47 |
| 48 | X.14 | X.15 | 48 | | | 48 |
| 49 | Y.0 | Y.1 | 49 | | | 49 |
| | | | | | | |
| 52 | Y.2 | Y.3 | 52 | | | 52 |
| 53 | Y.4 | Y.5 | 53 | | | 53 |
| 54 | Y.6 | Y.7 | 54 | | | 54 |
| 55 | Y.8 | Y.9 | 55 | | | 55 |
| 56 | Y.10 | Y.11 | 56 | | | 56 |
| 57 | Y.12 | Y.13 | 57 | | | 57 |
| 58 | Y.14 | Y.15 | 58 | | | 58 |
| 59 | YH.0 | YH.1 | 59 | | | 59 |
| 61 | YH.2 | YH.3 | 61 | | | 61 |
| 62 | YH.4 | YH.5 | 62 | | | 62 |
| 63 | YH.6 | YH.7 | 63 | | | 63 |
| 64 | Pt.0 | Pt.1 | 64 | | | 64 |
| 65 | Pt.2 | | 65 | | | 65 |
| 66 | Disp-Proc' | MemErr | 66 | | | 66 |
| 67 | DAddr.0 | DAddr.1 | 67 | | | 67 |
| 68 | DAddr.2 | DAddr.3 | 68 | | | 68 |
| 69 | DAddr.4 | DAddr.5 | 69 | | | 69 |
| 71 | DAddr.6 | DAddr.7 | 71 | | | 71 |
| 72 | DAddr.8 | DAddr.9 | 72 | | | 72 |
| 73 | DAddr.10 | DAddr.11 | 73 | | | 73 |
| 74 | DAddr.12 | DAddr.13 | 74 | | | 74 |
| 75 | DAddr.14 | DAddr.15 | 75 | | | 75 |
| 76 | DData.0 | DData.1 | 76 | | | 76 |
| 77 | DData.2 | DData.3 | 77 | | | 77 |
| 78 | DData.4 | DData.5 | 78 | | | 78 |
| 79 | DData.6 | DData.7 | 79 | | | 79 |
| 81 | DData.8 | DData.9 | 81 | | | 81 |
| 82 | DData.10 | DData.11 | 82 | | | 82 |
| 83 | DData.12 | DData.13 | 83 | | | 83 |
| 84 | DData.14 | DData.15 | 84 | | | 84 |
| 85 | SDI.20 | SDI.21 | 85 | SDI.20 | SDI.21 | 85 |
| 86 | SDI.18 | SDI.19 | 86 | SDI.18 | SDI.19 | 86 |
| 87 | SDI.16 | SDI.17 | 87 | SDI.16 | SDI.17 | 87 |
| 88 | SDI.14 | SDI.15 | 88 | SDI.14 | SDI.15 | 88 |
| 89 | SDI.12 | SDI.13 | 89 | SDI.12 | SDI.13 | 89 |
| 91 | SDI.10 | SDI.11 | 91 | SDI.10 | SDI.11 | 91 |
| 92 | SDI.08 | SDI.09 | 92 | SDI.08 | SDI.09 | 92 |
| 93 | SDI.06 | SDI.07 | 93 | SDI.06 | SDI.07 | 93 |
| 94 | SDI.04 | SDI.05 | 94 | SDI.04 | SDI.05 | 94 |
| 95 | SDI.02 | SDI.03 | 95 | SDI.02 | SDI.03 | 95 |
| 96 | SDI.00 | SDI.01 | 96 | SDI.00 | SDI.01 | 96 |
| | 1-100 | 101-200 | | 1-100 | 101-200 | |

Above diagram is rear view (wiring side) of backplane.
All numbers are in DECIMAL.

# Dandelion Backplane - 2

| Rev B | 2/19/80 |
|---|---|
| Ogus | 1:19 p |

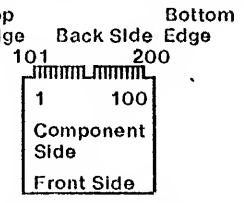
*Physical arrangement of cards:*




## Power & Ground

| Voltage | Pins |
|---|---|
| +12 V | 1,101 |
| +5 V | 50,51,150,151 |
| GND | 10,20,30,40,60 70,80,90,110,120, 130,140,160,170, 180,190 |
| -5 V | 100,200 |
| -12 V | 98,198 |
| No Conn | 97,99,197,199 |

## Card Edge Connector




2- 100 pin connectors
Pins on .1" centers
.6" between pins 50 & 51
2 - AMP # 530826-3

*Stamen5-6.sil In:*
*[Iris]<Workstation>Backplane>Backplane-B.dm*

| | IOP | | OPTIONS | | CP | | HSIO | | |
|---|---|---|---|---|---|---|---|---|---|
| 02 | | | Cycle.1' | Click.0 | Cycle1' | Click.0 | Cycle1' | Click.0 | 02 |
| 03 | | | Cycle.2' | Click.1 | Cycle2' | Click.1 | Cycle2' | Click.1 | 03 |
| 04 | | | Cycle.3' | Click.2 | Cycle3' | Click.2 | Cycle3' | Click.2 | 04 |
| 05 | Spare22 | Spare23 | Spare22 | Spare23 | | | RAS' | LRAS' | 05 |
| 06 | Spare2 | | Spare2 | | | | CAS | LCAS | 06 |
| 07 | Spare20 | Spare21 | Spare20 | Spare21 | Spare20 | Spare21 | WPulse | DR/C | 07 |
| 08 | Spare18 | Spare19 | Spare18 | Spare19 | Spare18 | Spare19 | | | 08 |
| 09 | ppCLK | | ppCLK | | ppCLK | | ppCLK | | 09 |
| 11 | Spare16 | Spare17 | Spare16 | Spare17 | AllowWrite | | AllowWrite | | 11 |
| 12 | IOPClk | | IOPClk | | | | | | 12 |
| 13 | Spare14 | Spare15 | Spare14 | Spare15 | MAR← | mem | MAR← | mem | 13 |
| 14 | Spare12 | Spare13 | Spare12 | Spare13 | | ←MStatus' | | ←MStatus' | 14 |
| 15 | IOPDataOut | BRClk | IOPDataOut | BRClk | MapRef | MCtl←' | MapRef | MCtl←' | 15 |
| 16 | SelTroyMode | Spare9 | SelTroyMode | Spare9 | Refresh' | | Refresh' | | 16 |
| 17 | Wait | IOPReset' | Wait | IOPReset' | Wait | IOPReset' | Wait | IOPReset' | 17 |
| 18 | TrIndex | TrHdLd | TrIndex | TrHdLd | Spare26 | Spare27 | Spare26 | Spare27 | 18 |
| 19 | TrReady | TrStep | TrReady | TrStep | Spare24 | Spare25 | Spare24 | Spare25 | 19 |
| 21 | IOPODData←' | IOPCtl←' | IOPODData←' | IOPCtl←' | IOPODData←' | IOPCtl←' | | | 21 |
| 22 | TrTK00 | TrDirIn | TrTK00 | TrDirIn | KOData←' | KCtl←' | KOData←' | KCtl←' | 22 |
| 23 | | | EOData←' | EICtl←' | EOData←' | EICtl←' | EOData←' | EICtl←' | 23 |
| 24 | TrWrProt | TrWrGate | TrWrProt | TrWrGate | DCtlFifo←' | DCtl←' | DCtlFifo←' | DCtl←' | 24 |
| 25 | TrRdData | TrWrData | TrRdData | TrWrData | DBorder←' | | DBorder←' | | 25 |
| 26 | EWrite' | EOCtl←' | EWrite' | EOCtl←' | EWrite' | EOCtl←' | EWrite' | EOCtl←' | 26 |
| 27 | KCmd←' | IOOutSp4←' | KCmd←' | IOOutSp4←' | KCmd←' | IOOutSp4←' | KCmd←' | IOOutSp4←' | 27 |
| 28 | | | PCData←' | PCtl←' | PCData←' | PCtl←' | PCData←' | PCtl←' | 28 |
| 29 | Spare6 | Spare7 | Spare6 | Spare7 | Spare6 | Spare7 | Spare6 | Spare7 | 29 |
| 31 | | | EIData' | EStatus' | EIData' | EStatus' | EIData' | EStatus' | 31 |
| 32 | Spare4 | Spare5 | Spare4 | Spare5 | ←KIData' | ←KStatus' | ←KIData' | ←KStatus' | 32 |
| 33 | | | | KWrite' | ←KTest' | KWrite' | ←KTest' | KWrite' | 33 |
| 34 | ←IOPIData' | ←IOPStatus' | ←IOPIData' | ←IOPStatus' | ←IOPIData' | ←IOPStatus' | | | 34 |
| 35 | ←IOInSp2' | | ←IOInSp2' | PrtReq' | ←IOInSp2' | PrtReq' | ←IOInSp2' | PrtReq' | 35 |
| 36 | IOPALE | Spare3 | IOPALE | Spare3 | IOPALE | Spare3 | IOPALE | Spare3 | 36 |
| 37 | CSParErr | | CSParErr | EndLine' | CSParErr | EndLine' | | EndLine' | 37 |
| 38 | IODisp.0 | IODisp.1 | IODisp.0 | IODisp.1 | IODisp.0 | IODisp.1 | IODisp.0 | IODisp.1 | 38 |
| 39 | YIODisp.0 | YIODisp.1 | YIODisp.0 | YIODisp.1 | YIODisp.0 | YIODisp.1 | YIODisp.0 | YIODisp.1 | 39 |
| 41 | X.0 | X.1 | X.0 | X.1 | X.0 | X.1 | X.0 | X.1 | 41 |
| 42 | X.2 | X.3 | X.2 | X.3 | X.2 | X.3 | X.2 | X.3 | 42 |
| 43 | X.4 | X.5 | X.4 | X.5 | X.4 | X.5 | X.4 | X.5 | 43 |
| 44 | X.6 | X.7 | X.6 | X.7 | X.6 | X.7 | X.6 | X.7 | 44 |
| 45 | X.8 | X.9 | X.8 | X.9 | X.8 | X.9 | X.8 | X.9 | 45 |
| 46 | X.10 | X.11 | X.10 | X.11 | X.10 | X.11 | X.10 | X.11 | 46 |
| 47 | X.12 | X.13 | X.12 | X.13 | X.12 | X.13 | X.12 | X.13 | 47 |
| 48 | X.14 | X.15 | X.14 | X.15 | X.14 | X.15 | X.14 | X.15 | 48 |
| 49 | | | Y.0 | Y.1 | Y.0 | Y.1 | Y.0 | Y.1 | 49 |
| 52 | | | Y.2 | Y.3 | Y.2 | Y.3 | Y.2 | Y.3 | 52 |
| 53 | | | Y.4 | Y.5 | Y.4 | Y.5 | Y.4 | Y.5 | 53 |
| 54 | | | Y.6 | Y.7 | Y.6 | Y.7 | Y.6 | Y.7 | 54 |
| 55 | | | Y.8 | Y.9 | Y.8 | Y.9 | Y.8 | Y.9 | 55 |
| 56 | | | Y.10 | Y.11 | Y.10 | Y.11 | Y.10 | Y.11 | 56 |
| 57 | | | Y.12 | Y.13 | Y.12 | Y.13 | Y.12 | Y.13 | 57 |
| 58 | | | Y.14 | Y.15 | Y.14 | Y.15 | Y.14 | Y.15 | 58 |
| 59 | DmaReqC' | DmaAckC' | DmaReqC' | DmaAckC' | YH.0 | YH.1 | YH.0 | YH.1 | 59 |
| 61 | DmaReqA' | DmaAckA' | DmaReqA' | DmaAckA' | YH.2 | YH.3 | YH.2 | YH.3 | 61 |
| 62 | DmaReqB' | DmaAckB' | DmaReqB' | DmaAckB' | YH.4 | YH.5 | YH.4 | YH.5 | 62 |
| 63 | DmaCycle | ExtWaitReq' | DmaCycle | ExtWaitReq' | YH.6 | YH.7 | YH.6 | YH.7 | 63 |
| 64 | IOPIntReq0 | IOPIntReq1 | IOPIntReq0 | IOPIntReq1 | Pt.0 | Pt.1 | Pt.0 | Pt.1 | 64 |
| 65 | IOPIntReq2 | IOPIntReq3 | IOPIntReq2 | IOPIntReq3 | Pt.2 | | Pt.2 | | 65 |
| 66 | IOPSel.0' | IOPSel.1' | IOPSel.0' | IOPSel.1' | Disp-Proc' | MemErr | Disp-Proc' | MemErr | 66 |
| 67 | IOPSel.2' | IOPSel.3' | IOPSel.2' | IOPSel.3' | | | DAddr.0 | DAddr.1 | 67 |
| 68 | IOPSel.4' | IOPSel.5' | IOPSel.4' | IOPSel.5' | | | DAddr.2 | DAddr.3 | 68 |
| 69 | IOPAddr.00 | IOPAddr.01 | IOPAddr.00 | IOPAddr.01 | | | DAddr.4 | DAddr.5 | 69 |
| 71 | IOPAddr.02 | IOPAddr.03 | IOPAddr.02 | IOPAddr.03 | | | DAddr.6 | DAddr.7 | 71 |
| 72 | IOPAddr.04 | IOPAddr.05 | IOPAddr.04 | IOPAddr.05 | | | DAddr.8 | DAddr.9 | 72 |
| 73 | IOPAddr.06 | IOPAddr.07 | IOPAddr.06 | IOPAddr.07 | | | DAddr.10 | DAddr.11 | 73 |
| 74 | IOPAddr.08 | IOPAddr.09 | IOPAddr.08 | IOPAddr.09 | | | DAddr.12 | DAddr.13 | 74 |
| 75 | IOPAddr.10 | IOPAddr.11 | IOPAddr.10 | IOPAddr.11 | | | DAddr.14 | DAddr.15 | 75 |
| 76 | IOPAddr.12 | IOPAddr.13 | IOPAddr.12 | IOPAddr.13 | IOPAddr.12 | IOPAddr.13 | DData.0 | DData.1 | 76 |
| 77 | IOPAddr.14 | IOPAddr.15 | IOPAddr.14 | IOPAddr.15 | IOPAddr.14 | IOPAddr.15 | DData.2 | DData.3 | 77 |
| 78 | Spare0 | Spare1 | Spare0 | Spare1 | Spare0 | Spare1 | DData.4 | DData.5 | 78 |
| 79 | IOPMemRd' | IOPI/ORd' | IOPMemRd' | IOPI/ORd' | | | DData.6 | DData.7 | 79 |
| 81 | CSWE.a' | CSWE.b' | CSWE.a' | CSWE.b' | CSWE.a' | CSWE.b' | DData.8 | DData.9 | 81 |
| 82 | CSWE.c' | CSWE.d' | CSWE.c' | CSWE.d' | CSWE.c' | CSWE.d' | DData.10 | DData.11 | 82 |
| 83 | CSWE.e' | CSWE.f' | CSWE.e' | CSWE.f' | CSWE.e' | CSWE.f' | DData.12 | DData.13 | 83 |
| 84 | IOPReq' | ClrIOPReq' | IOPReq' | ClrIOPReq' | IOPReq' | ClrIOPReq' | DData.14 | DData.15 | 84 |
| 85 | | | DPReq' | ClrDPReq' | DPReq' | ClrDPReq' | DPReq' | ClrDPReq' | 85 |
| 86 | | | EReq' | ClrRefReq' | EReq' | ClrRefReq' | EReq' | ClrRefReq' | 86 |
| 87 | IOPMemWr' | IOPI/OWr' | IOPMemWr' | IOPI/OWr' | KReq' | ClrKFlags' | KReq' | ClrKFlags' | 87 |
| 88 | RefReq' | ReadCSEn' | RefReq' | ReadCSEn' | RefReq' | ReadCSEn' | RefReq' | | 88 |
| 89 | EORound | IOPWait | EORound | IOPWait | EORound | IOPWait | EORound | | 89 |
| 91 | WrTPCHigh' | WrTPCLow | WrTPCHigh' | WrTPCLow | WrTPCHigh' | WrTPCLow | | | 91 |
| 92 | IOPData.0 | IOPData.1 | IOPData.0 | IOPData.1 | IOPData.0 | IOPData.1 | | | 92 |
| 93 | IOPData.2 | IOPData.3 | IOPData.2 | IOPData.3 | IOPData.2 | IOPData.3 | | | 93 |
| 94 | IOPData.4 | IOPData.5 | IOPData.4 | IOPData.5 | IOPData.4 | IOPData.5 | | | 94 |
| 95 | IOPData.6 | IOPData.7 | IOPData.6 | IOPData.7 | IOPData.6 | IOPData.7 | | | 95 |
| 96 | SwTAddr | SwTAddr' | SwTAddr | SwTAddr' | SwTAddr | SwTAddr' | | | 96 |
| | 1-100 | 101-200 | 1-100 | 101-200 | 1-100 | 101-200 | 1-100 | 101-200 | |

Above diagram is rear view (wiring side) of backplane.
ALL NUMBERS ARE IN DECIMAL.

# Dandelion Backplane Signals - 1

*Stamen1-4.sil in: [Iris]<Workstation>Backplane>Backplane-C.dm*

| Rev C | 9/26/80 |
|---|---|
| Ogus | |

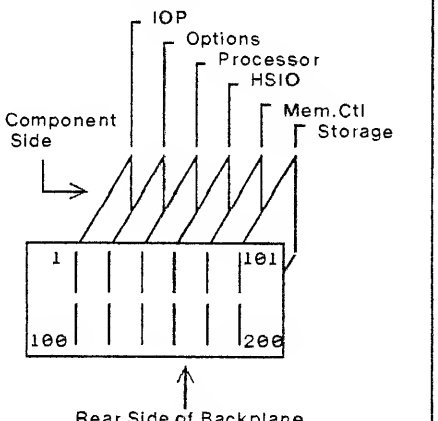
| | MEM CTRL | | STORAGE | | |
|---|---|---|---|---|---|
| 02 | Cycle1' | | 02 | | 02 |
| 03 | Cycle2' | | 03 | | 03 |
| 04 | Cycle3' | | 04 | | 04 |
| 05 | RAS' | LRAS' | 05 | RAS' | LRAS' 05 |
| 06 | CAS | LCAS | 06 | CAS | LCAS 06 |
| 07 | WPulse | DR/C | 07 | | 07 |
| 08 | | | 08 | | 08 |
| 09 | ppCLK | | 09 | ppCLK | 09 |
| 11 | AllowWrite | | 11 | | 11 |
| 12 | Bank0' | | 12 | Bank0' | 12 |
| 13 | MAR← | mem | 13 | | 13 |
| 14 | | ←MStatus' | 14 | | 14 |
| 15 | MapRef | MCtl←' | 15 | | 15 |
| 16 | Refresh' | CRefresh' | 16 | Refresh' | CRefresh' 16 |
| 17 | Wait | | 17 | | 17 |
| 18 | SDO.00 | SDO.01 | 18 | SDO.00 | SDO.01 18 |
| 19 | SDO.02 | SDO.03 | 19 | SDO.02 | SDO.03 19 |
| 21 | SDO.04 | SDO.05 | 21 | SDO.04 | SDO.05 21 |
| 22 | SDO.06 | SDO.07 | 22 | SDO.06 | SDO.07 22 |
| 23 | SDO.08 | SDO.09 | 23 | SDO.08 | SDO.09 23 |
| 24 | SDO.10 | SDO.11 | 24 | SDO.10 | SDO.11 24 |
| 25 | SDO.12 | SDO.13 | 25 | SDO.12 | SDO.13 25 |
| 26 | SDO.14 | SDO.15 | 26 | SDO.14 | SDO.15 26 |
| 27 | SDO.16 | SDO.17 | 27 | SDO.16 | SDO.17 27 |
| 28 | SDO.18 | SDO.19 | 28 | SDO.18 | SDO.19 28 |
| 29 | SDO.20 | SDO.21 | 29 | SDO.20 | SDO.21 29 |
| 31 | | | 31 | | 31 |
| 32 | SAddr.00 | SAddr.01 | 32 | SAddr.00 | SAddr.01 32 |
| 33 | SAddr.02 | SAddr.03 | 33 | SAddr.02 | SAddr.03 33 |
| 34 | SAddr.04 | SAddr.05 | 34 | SAddr.04 | SAddr.05 34 |
| 35 | SAddr.06 | SAddr.07 | 35 | SAddr.06 | SAddr.07 35 |
| 36 | Y1Latch | YOLatch | 36 | Y1Latch | YOLatch 36 |
| 37 | Bank1' | Bank2' | 37 | Bank1' | Bank2' 37 |
| 38 | MRef' | Write' | 38 | MRef' | Write' 38 |
| 39 | | | 39 | | 39 |
| 41 | X.0 | X.1 | 41 | | 41 |
| 42 | X.2 | X.3 | 42 | | 42 |
| 43 | X.4 | X.5 | 43 | | 43 |
| 44 | X.6 | X.7 | 44 | | 44 |
| 45 | X.8 | X.9 | 45 | | 45 |
| 46 | X.10 | X.11 | 46 | | 46 |
| 47 | X.12 | X.13 | 47 | | 47 |
| 48 | X.14 | X.15 | 48 | | 48 |
| 49 | Y.0 | Y.1 | 49 | | 49 |
| | | | | | |
| 52 | Y.2 | Y.3 | 52 | | 52 |
| 53 | Y.4 | Y.5 | 53 | | 53 |
| 54 | Y.6 | Y.7 | 54 | | 54 |
| 55 | Y.8 | Y.9 | 55 | | 55 |
| 56 | Y.10 | Y.11 | 56 | | 56 |
| 57 | Y.12 | Y.13 | 57 | | 57 |
| 58 | Y.14 | Y.15 | 58 | | 58 |
| 59 | YH.0 | YH.1 | 59 | | 59 |
| 61 | YH.2 | YH.3 | 61 | | 61 |
| 62 | YH.4 | YH.5 | 62 | | 62 |
| 63 | YH.6 | YH.7 | 63 | | 63 |
| 64 | Pt.0 | Pt.1 | 64 | | 64 |
| 65 | Pt.2 | | 65 | | 65 |
| 66 | Disp-Proc' | MemErr | 66 | | 66 |
| 67 | DAddr.0 | DAddr.1 | 67 | | 67 |
| 68 | DAddr.2 | DAddr.3 | 68 | | 68 |
| 69 | DAddr.4 | DAddr.5 | 69 | | 69 |
| 71 | DAddr.6 | DAddr.7 | 71 | | 71 |
| 72 | DAddr.8 | DAddr.9 | 72 | | 72 |
| 73 | DAddr.10 | DAddr.11 | 73 | | 73 |
| 74 | DAddr.12 | DAddr.13 | 74 | | 74 |
| 75 | DAddr.14 | DAddr.15 | 75 | | 75 |
| 76 | DData.0 | DData.1 | 76 | | 76 |
| 77 | DData.2 | DData.3 | 77 | | 77 |
| 78 | DData.4 | DData.5 | 78 | | 78 |
| 79 | DData.6 | DData.7 | 79 | | 79 |
| 81 | DData.8 | DData.9 | 81 | | 81 |
| 82 | DData.10 | DData.11 | 82 | | 82 |
| 83 | DData.12 | DData.13 | 83 | | 83 |
| 84 | DData.14 | DData.15 | 84 | | 84 |
| 85 | SDI.20 | SDI.21 | 85 | SDI.20 | SDI.21 85 |
| 86 | SDI.18 | SDI.19 | 86 | SDI.18 | SDI.19 86 |
| 87 | SDI.16 | SDI.17 | 87 | SDI.16 | SDI.17 87 |
| 88 | SDI.14 | SDI.15 | 88 | SDI.14 | SDI.15 88 |
| 89 | SDI.12 | SDI.13 | 89 | SDI.12 | SDI.13 89 |
| 91 | SDI.10 | SDI.11 | 91 | SDI.10 | SDI.11 91 |
| 92 | SDI.08 | SDI.09 | 92 | SDI.08 | SDI.09 92 |
| 93 | SDI.06 | SDI.07 | 93 | SDI.06 | SDI.07 93 |
| 94 | SDI.04 | SDI.05 | 94 | SDI.04 | SDI.05 94 |
| 95 | SDI.02 | SDI.03 | 95 | SDI.02 | SDI.03 95 |
| 96 | SDI.00 | SDI.01 | 96 | SDI.00 | SDI.01 96 |
| | 1-100 | 101-200 | | 1-100 | 101-200 |

Above diagram is rear view (wiring side) of backplane.
All numbers are in DECIMAL.

# Dandelion Backplane - 2

| Rev C | 9/26/80 |
|---|---|
| Ogus | |

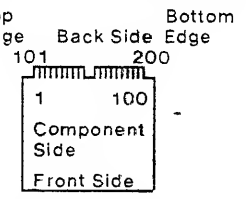
*Physical arrangement of cards:*




## Power & Ground

| Voltage | Pins |
|---|---|
| +12 V | 1,101 |
| +5 V | 50,51,150,151 |
| GND | 10,20,30,40,60 70,80,90,110,120, 130,140,160,170, 180,190 |
| -5 V | 100,200 |
| -12 V | 98,198 |
| No Conn | 97,99,197,199 |

## Card Edge Connector




2- 100 pin connectors
Pins on .1" centers
.6" between pins 50 & 51
2- AMP # 530826-3

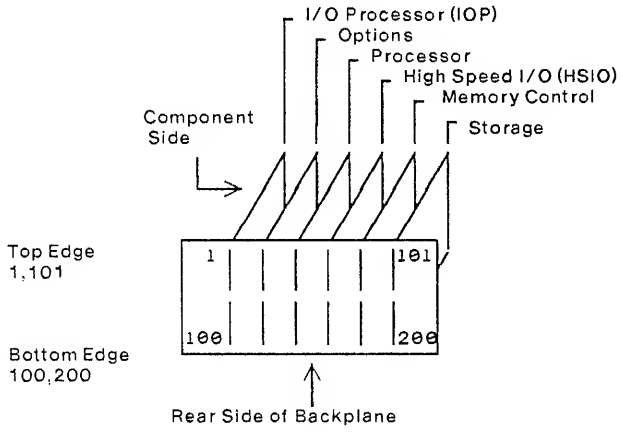
*Stamen5-6.sil in:*
*[Iris]<Workstation>Backplane>Backplane-C.dm*

## *Revision B to Revision C*

- Rename XOData←' to EOData←' (23 )
- Rename XCtl←' to ElCtl←' (123 )
- Rename IOOutSp1←' to EWrite' ( 26 )
- Rename IOOutSp2←' to EOCtl←' (126 )
- Rename IOOutSp3←' to KCmd←' (27 )
- Rename ←XIData' to ElData' (31 )
- Rename ←XStatus' to EStatus' (131 )
- Rename ←PStatus' to KWrite' ( 133 )
- Rename XReq' to EReq' (86 )
- Rename ClrXReq' to ClrRefReq' ( 186 )
- Rename SpareReq' to EORound (89 )
- Rename Spare10 to IOPDataOut (15 )
- Rename Spare11 to BRClk ( 115 )
- Rename ClrRefReq' to PrtReq' (135 )
- Rename Spare2 to IOPALE ( 36 )
- Rename IOPALE to Spare2 (06 )
- Rename DmaReqA to DmaReqA' ( 61 )
- Rename DmaReqB to DmaReqB' ( 62 )
- Rename DmaReqC to DmaReqC' ( 59 )
- Rename DmaAckA to DmaAckA' (161 )
- Rename DmaAckB to DmaAckB' (162 )
- Rename DmaAckC to DmaAckC' (159 )
- rename IOPSel.0 to IOIPSel.0' ( 66 )
- rename IOPSel.1 to IOIPSel.1' ( 166 )
- rename IOPSel.2 to IOIPSel.2' ( 67 )
- rename IOPSel.3 to IOIPSel.3' (167 )
- rename IOPSel.4 to IOIPSel.4' ( 68 )
- rename IOPSel.5 to IOIPSel.5' (168 )

# Dandelion Backplane

## Physical arrangement




## Files

[Iris]<Workstation>Backplane>
Backplane-C.press
Backplane-C.dm

## Backplane Signals

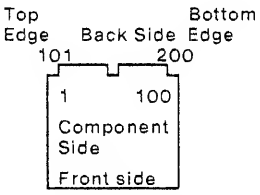
| Card | IOP | Options | Central Processor | High Speed I/O | Memory Control | Storage |
|---|---|---|---|---|---|---|
| Total Signal lines used | 131 | 166 | 140 | 141 | 155 | 66 |

170 max. per card

| I/O Connectors on front of boards | | | | | | |
|---|---|---|---|---|---|---|
| | Floppy<br>Keyboard<br>Printer<br>MaintenanceP<br>Alto umb. | LSEP/Ethernet<br>RS232/RS366 | | SA4XXX<br>SA100X<br>Display | | |

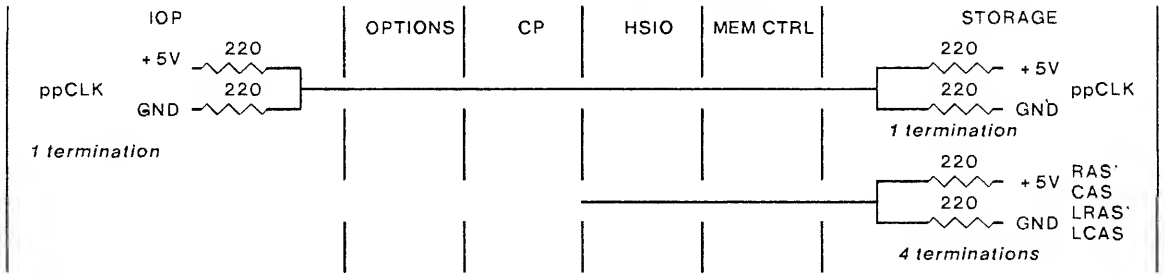
## Power distribution

| Backplane Power & Ground | 30 lines total |
|---|---|
| Voltage | Backplane Pins |
| + 12 V | 1,101 |
| + 5 V | 50.51.150,151 |
| Gnd | 10.20.30,40,60.70.80.90,110,120,130.140.160,170.180,190 |
| - 5V | 100.200 |
| - 12 V | 98,198 |
| No Conn. | 97,99,197,199 |




2- 100 pin connectors
Pins on .1" centers
.6" between pins 50 & 51
AMP # 530826-3

## Termination of clock signals




Terminations are placed on the IOP and STORAGE cards.

| XEROX SDD | Project | Backplane Description | File | Designer | Rev | Date |
|---|---|---|---|---|---|---|
| | Dandelion | General Characteristics | WSBackplane.sil | Ogus | C | 9/26/80 |